16th International Workshop on Cellular Nanoscale Networks and their Applications (CNNA) and 6th Memristor and Memristive Symposium (MMS)

August 27-30, 2018

Budapest, Hungary

Conference Guide

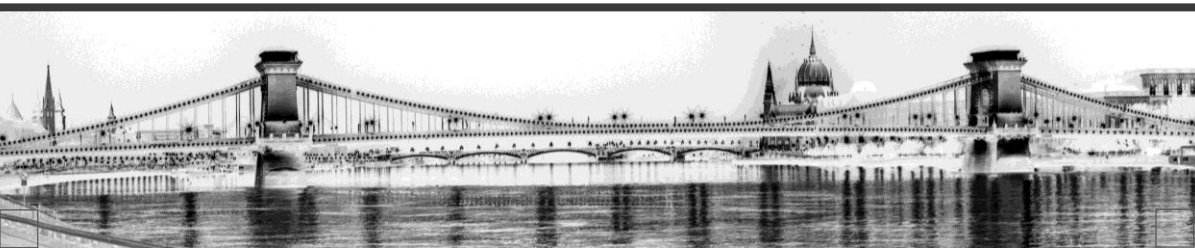
Organizers:

Pázmány Péter Catholic University

Institute of Computer Science and Control, HAS

General Chair:

Péter Szolgay
Pázmány Péter Catholic University



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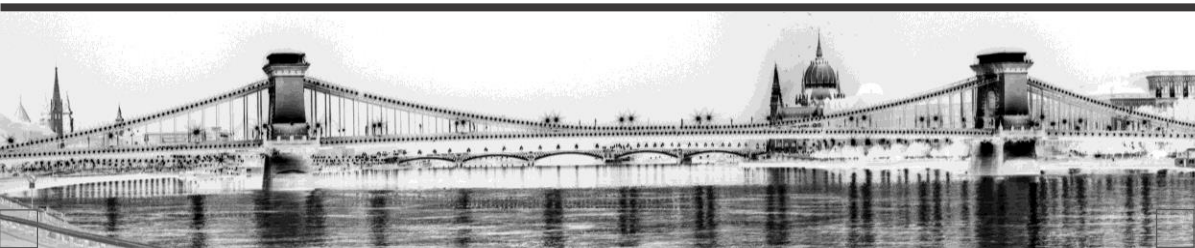

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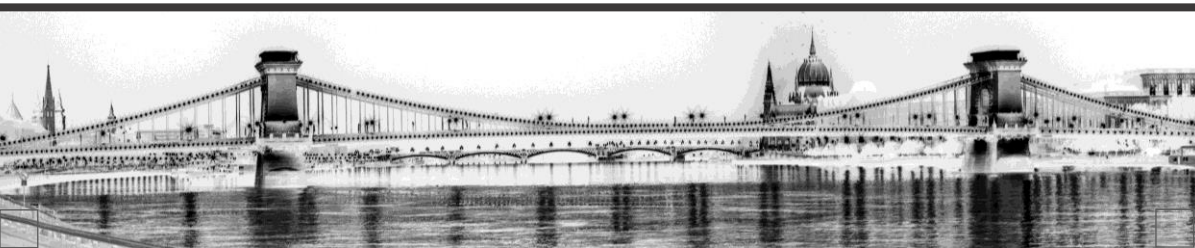

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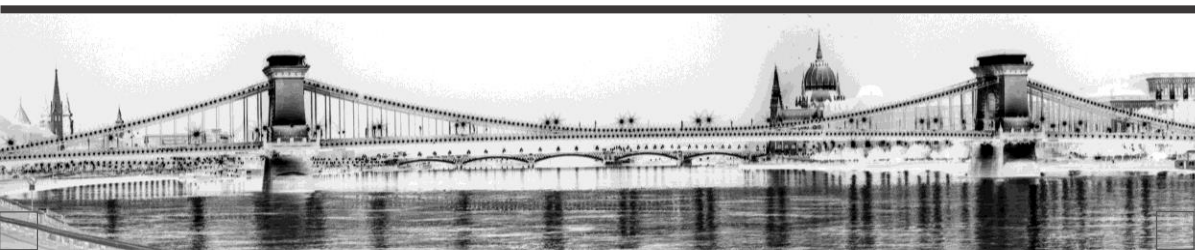


Dear Friends, welcome to Budapest!

It is my distinguished pleasure to express a warm welcome on behalf of the Organizing Committee and of the Scientific Committee to all participants of the 6th Memristor and Memristive Symposium (MMS) and the 16th International Workshop on Cellular Nanoscale Network and their Applications (CNNA).

These scientific events are sponsored by Pázmány Péter Catholic University, Institute of Computer Science and Control of the Hungarian Academy of Sciences and technically co-sponsored by the Institute of Electrical and Electronic Engineers (IEEE) and the Office of Naval Research Global (ONR Global).

The Memristor and Memristive Symposium and the International Workshop on Cellular Nanoscale Networks and their Applications have been organized all over the world. While MMS followed a biennial series of Symposia subsequently hosted in Berkeley (2008, 2010), Turin (2012) Notre Dame (2014) and Dresden (2016), the CNNA was hosted in Budapest (1990), Munich (1992), Rome (1994), Seville (1996), London (1998), Catania (2000), Frankfurt/Main (2002), Budapest (2004), Hsichu (2005), Istanbul (2006), Santiago de Compostela (2008), Berkeley (2010), Turin (2012), Notre Dame (2014) and Dresden (2016). These events proved to be successful in bringing together scientists from different research areas and exploiting the results of different applications.

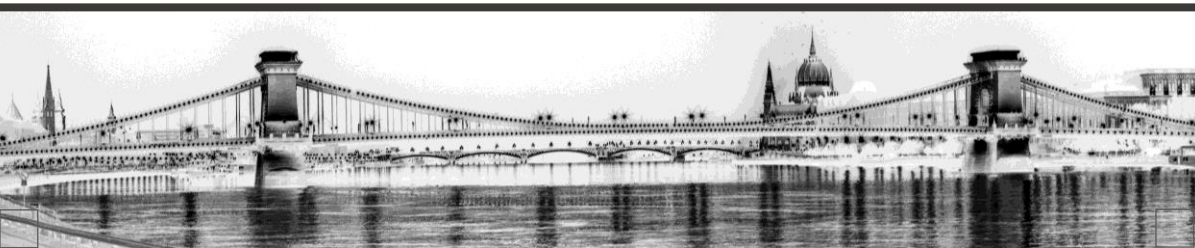
The Program Chair with the active help of members of the Scientific Committee did a very careful review of the submitted contributions.

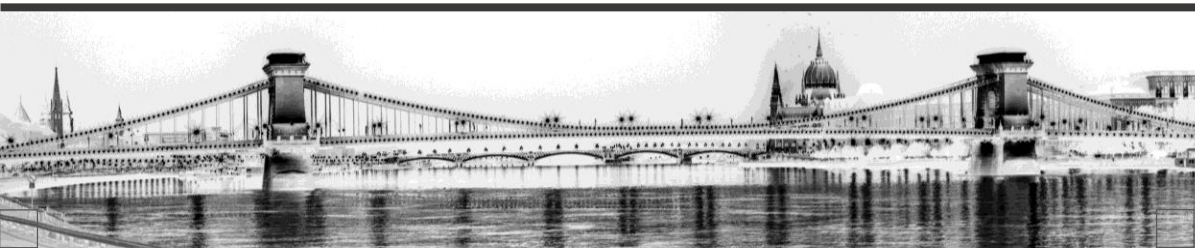
The program of the 6th MMS presents plenary lectures of Prof. Leon O. Chua, Dr. Geoffrey W. Burr, Prof. D. Ielmini, Prof. Wei Lu, Prof. Ming Lu, Prof. Ronald Tetzlaff, Prof. Jianhua Yang, Prof. Fernando Corinto, Dr. Vikas Rana, Prof. Nikolay V. Kuznetsov and Prof. Giorgos Sirakoulis. As far as the program of the 16th CNNA Workshop is considered there are 6 sessions, a demo session and the plenary lectures of Prof. Wolfgang Porod, Prof. Angel Rodriguez-Vázquez and András Horváth.

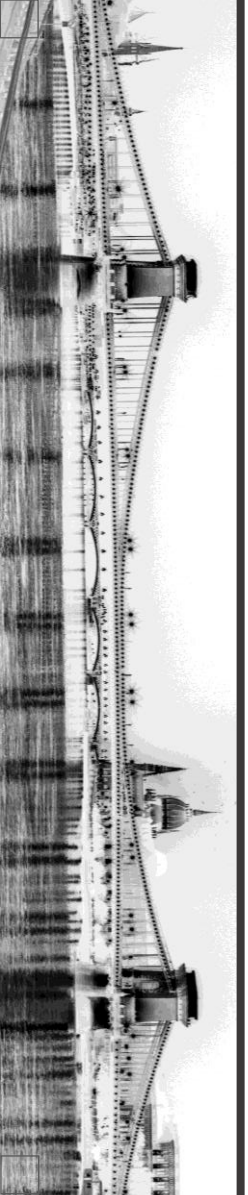
I would like to thank all of sponsoring organizations and all who helped to make the 6th Memristor and Memristive Symposium and the 16th International Workshop on Cellular Nanoscale Networks and their Applications possible.

I wish all of you a very pleasant stay opening new directions in Budapest.

Péter Szolgay



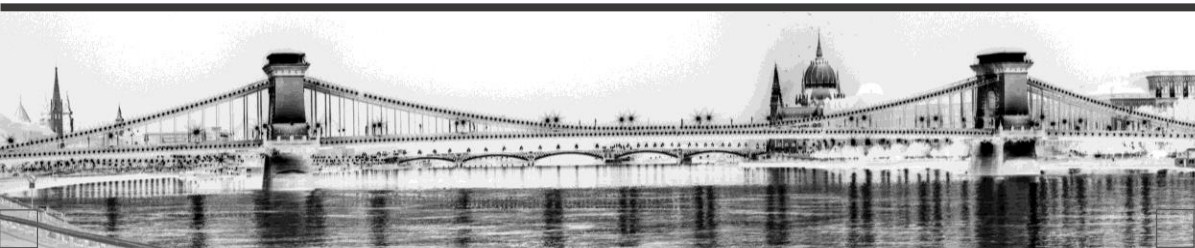




August 27	August 28	August 29	August 30
Memristor Symposium	CNNA		
9:00-11:00 Leon O. Chua 11:00-11:15 *Coffee break* 11:15-11:45 Daniele Ielmini 11:45-12:30 Geoffrey W. Burr 12:30-13:00 Ming Liu 13:00-14:15 *Lunch* 14:15-14:45 Ronald Tetzlaff 14:45-15:15 Zhongrui Wang 15:15-15:45 Fernando Corinto 15:45-16:00 *Coffee break* 16:00-16:30 Vikas Rana 16:30-17:00 Nikolay V. Kuznetsov 17:00-17:30 Georgios Sirakoulis	9:00-9:15 Welcome 9:15-10:05 Plenary talk Angel Rodriguez- Vazquez 10:05-10:30 *Coffee break* 10:30-12:50 TS1.1. Beyond Moore Implementations: Memristors and Oscillators 12:50-14:00 *Lunch* 14:00-15:40 TS1.2. Medical Applications 15:40-16:00 *Coffee break* 16:00-17:40 TS1.3. Cameras, Architectures and VLSI Implementation	9:00-9:50 Plenary talk Andras Horvath 9:50-10:20 *Coffee break* 10:20-12:00 TS2.1. Applications 12:00-13:10 *Lunch* 13:10-14:50 TS2.2. FPGA Implementations 14:50-16:00 Demo session 14:50-16:00 *Coffee break*	9:00-9:50 Plenary talk Wolfgang Porod 9:50-10:05 *Coffee break* 10:05-11:45 TS3.1. Network Theory and Learning 11:45 *Lunch*
17.45 Opening reception		16:00 Buses leave to Esztergom sightseeing and concert	

MEMRISTOR SYMPOSIUM – AUGUST 27

9:00 - 11:00	**Opening of Symposium** **Prof. Leon O. Chua:** *Five Non-Volatile Memristor Enigmas Solved*
11:00 - 11:15	break
11:15 - 11:45	**Prof. Daniele Ielmini:** *Brain-inspired computing with resistive switching memory devices*
11:45 - 12:30	**Geoffrey W. Burr:** *Memristor requirements for Accelerating Deep Neural Networks with Analog Memory*
12:30 - 13:00	**Prof. Ming Liu:** *RRAM for Future Memory and Computing Application*
13:00 - 14:15	lunch
14:15 - 14:45	**Prof. Ronald Tetzlaff:** *In-Memory computing based on complex behavior in memristor circuits*
14:45 - 15:15	**Prof. Zhongrui Wang:** *Diffusive Memristors For Computing*
15:15 - 15:45	**Prof. Fernando Corinto:** *Analog Computing with Networks of Memristors Oscillators*
15:45 - 16:00	break
16:00 -16:30	**Dr. Vikas Rana:** *Forming Free ReRAM Devices and its application beyond Data Storage*
16:30 - 17:00	**Prof. Nikolay V. Kuznetsov:** *Complex dynamics and multistability in nonlinear electronic circuits and memristive systems*
17:00 - 17:30	**Dr. Georgios Sirakoulis:** *The Memristive Cellular Automata Computing Paradigm: Emergent Applications and Future Trends*
17.45	**Opening reception**



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Speakers

Prof. Leon O. Chua
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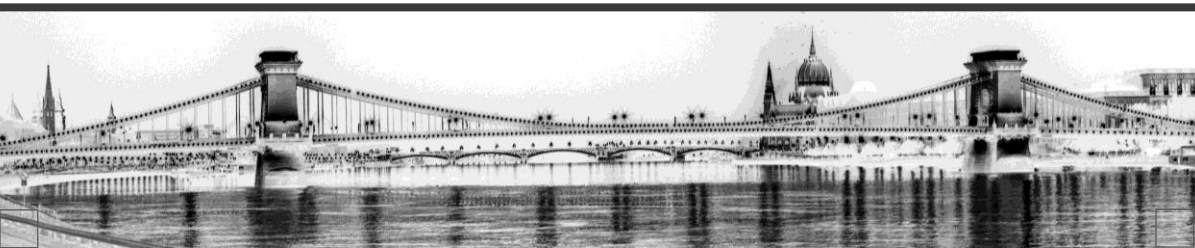
Five Non-Volatile Memristor Enigmas Solved

POP and DRM are fundamental concepts needed to understand why the memory-device community's cornucopia of acronyms of non-volatile resistive switching memories (such as RRAM, MRAM, Ferro-electric RAM, STT-RAM, ReRAM, PCM (Phase Change Memory, etc.,)) are mere examples of memristors.

POP and DRM are the mathematical properties that determine whether a memristor is volatile or non-volatile. Among other things, POP and DRM are the keys to prove and explain the following hitherto unresolved mysteries:

- All non-volatile memristors are continuum (analog) memories.
- All non-volatile memristors can be switched from one state to another by a square pulse, whose minimum amplitude and minimum width are constrained by a hyperbolic-like law.
- All non-volatile memristors driven by a single-polarity periodic voltages $0 \leq |v(t)| \leq A$ must exhibit a multi-prong finger-like pinched hysteresis loci in the I vs. V plane.

All non-volatile memristors do not have a DC V-I curves.



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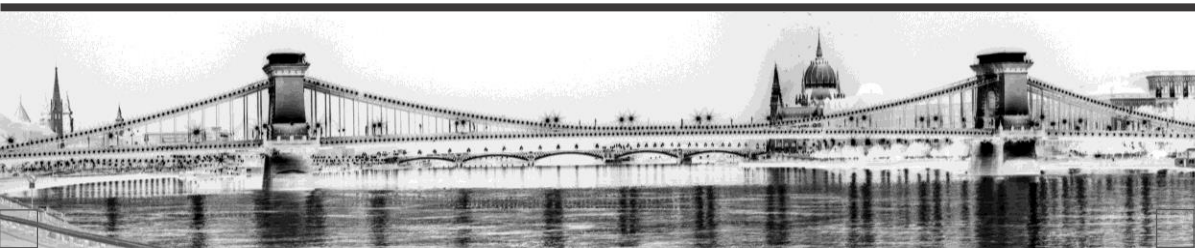
Memristor requirements for Accelerating Deep Neural Networks with Analog Memory

Deep Neural Networks (DNNs) are very large artificial neural networks trained using very large datasets, typically using the supervised learning technique known as backpropagation. Currently, CPUs and GPUs are used for these computations. Over the next few years, we can expect special-purpose hardware accelerators based on conventional digital-design techniques to optimize the GPU framework for these DNN computations. Here there are opportunities to increase speed and reduce power for two distinct but related tasks: training and forward-inference. During training, the weights of a DNN are adjusted to improve network performance through repeated exposure to the labelled data-examples of a large dataset. Often this involves a distributed network of chips working together in the cloud. During forward-inference, already trained networks are used to analyze new data-examples, sometimes in a latency-constrained cloud environment and sometimes in a power-constrained environment (sensors, mobile phones, "edge-of-network" devices, etc.)

Even after the improved computational performance and efficiency that is expected from these special-purpose digital accelerators, there would still be an opportunity for even higher performance and even better energy-efficiency from neuromorphic computation based on analog memories (including, potentially, memristors).

In this presentation, I discuss the origin of this opportunity as well as the challenges inherent in delivering on it, with some focus on materials and devices for analog volatile and non-volatile memory. I review our group's work towards neuromorphic chips for the hardware acceleration of training and inference of Fully-Connected DNNs [1-5]. Our group uses arrays of emerging



non-volatile memories (NVM), such as Phase Change Memory, to implement the synaptic weights connecting layers of neurons. I will discuss the impact of real device characteristics – such as non-linearity, variability, asymmetry, and stochasticity – on performance, and describe how these effects determine the desired specifications for the analog resistive memories needed for this application. I present some novel solutions to finesse some of these issues in the near-term, and describe some challenges in designing and implementing the CMOS circuitry around the NVM array. I will end with an outlook on the prospects for analog memory-based DNN hardware accelerators.

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Prof. Daniele Ielmini, G. Pedretti, W. Wang, V. Milo, E. Ambrosi, S. Bianchi, A. Bricalli, R. Carboni, I. Munoz, Z. Sun
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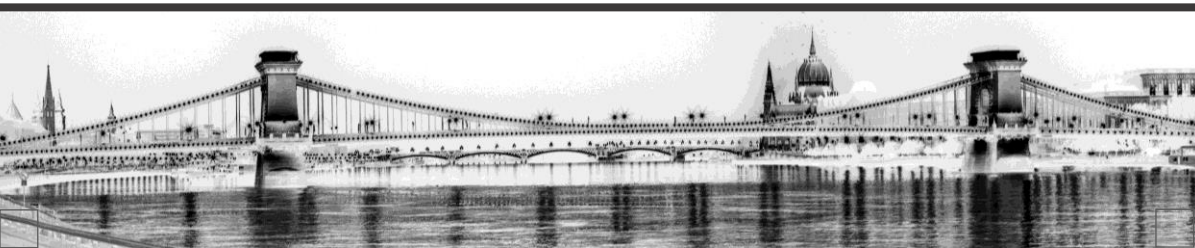
Brain-inspired computing with resistive switching memory devices

The rise of big data has motivated the search of novel computing architectures capable of in-memory, data centric processing of large unstructured data. To this aim, resistive memories, such as the resistive switching memory (RRAM) and the phase change memory (PCM), are extremely promising for their ability to store multivalued data, switch at high speed, and combine computation and memory in one device. Recently, synaptic circuits based on RRAM and PCM have been developed, demonstrating the ability to perform biological learning rules, such as the spike timing dependent plasticity (STDP) and the spike-rate dependent plasticity (SRDP). The potential breakthrough of in-memory synaptic computation however remains largely unexplored to date.



This talk will provide an overview of the recent achievements in developing brain-inspired cognitive computing primitives in hardware thanks to RRAM and PCM synapses. The general structure of a spiking neural network (SNN) with resistive synapses, and the self-learning functionality in the network will be presented, demonstrating feedforward learning, associative memories in recurrent networks, and spatio-temporal pattern learning. The relevance of the developed functions for emulating human-brain cognitive functions will be discussed.

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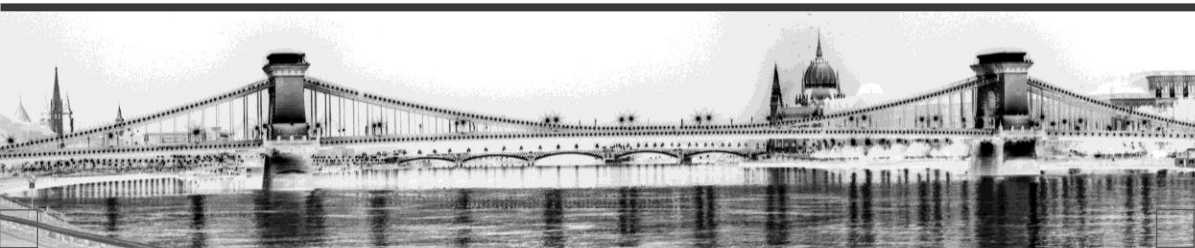
Memristor-based computing: from devices to systems

Memristors and memristive devices have now been extensively studied for memory and neuromorphic computing applications. These devices merge electronics with ionics to directly modulate the materials' internal atomic configuration, thus allowing the material properties to be controlled in-situ in a non-volatile yet reversible fashion. In this talk, I will discuss our efforts on the development and optimization of memristor devices and integrated systems, including techniques of controlling the dynamic ionic migration processes and associated modeling efforts. Functional high-density crossbar arrays have been integrated directly on top of CMOS circuits using a back-end-of-line (BEOL) process, enabling hybrid non-volatile memory and logic applications. Properly tuned devices also exhibit internal dynamics that are analogous to those observed in biological systems and allow the system to faithfully emulate biological neural networks. Prototype neuromorphic circuits based on memristor arrays have been shown to be able to perform tasks such as pattern recognition and image processing in an unsupervised fashion for intelligent sensing and analysis, and can be extended to other data intensive applications.



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RRAM for Future Memory and Computing Application

Benefit from IC aggressive progress in past 60 decades, computing system's performance has improved 1010 times. As the Moore's law slow down and the Von Neumann architecture's limitation, further performance's enhancement is increasingly constrained. Emerging memory technologies such as resistive RAM (RRAM) are being explored as potential alternatives to existing memories in future computing systems. Especially, due to the excellent compatibility with CMOS process and ease of 3D integration, RRAM provides a promising potential for embedded and standalone application as well as in memory computing. In this talk, current status, challenges and future trends of RRAM technology will be discussed.

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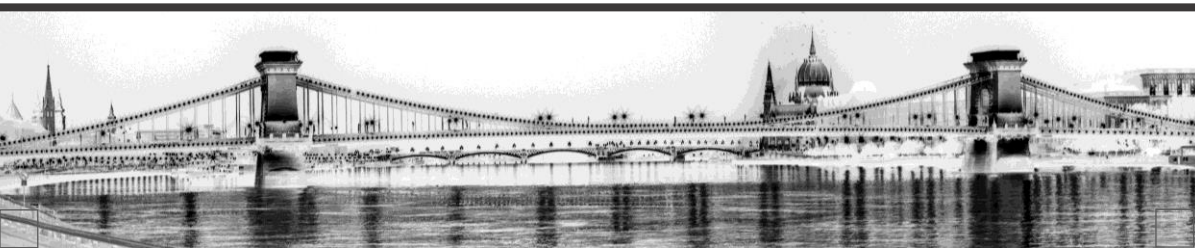
In-Memory computing based on complex behavior in memristor circuits

The development of future computing systems allowing the implementation of sensor-processor structures is addressed in various recent investigations in order to overcome the limits of conventional von Neumann architectures. Although, new developments have been made by endowing certain processors with memory systems, the implementation of time- and power-efficient programmable computing architectures on board of sensors remains an open



problem. Thereby, structures that use coupled memory cells in order to process and store data on the same physical platform have been proposed to provide a novel paradigm for IoT machines and Cyber Physical Systems. CMOS computing implementations of cellular networks have been applied in several applications to demonstrate their huge potential for future electronics. Especially, the complex behaviour emerging in these networks have been considered to solve multidimensional signal processing and classification problems. Hereby, wave propagation phenomena in these spatiotemporal systems and oscillatory solutions are exploited to solve problems under conditions in practice. Especially, Chua [1] has shown that the emergence of complex behavior in nonlinear dynamical arrays is based on local activity and especially on a parameter subset called the "Edge of Chaos (EOC)".

In this contribution, in order to overcome the limits posed by conventional CMOS technology, the emergence complex behavior of locally coupled Niobium oxide based memristor circuits will be addressed. The derivation of the EOC parameter subset based on an accurate compact model of a Niobium device [2,3] will be presented and solutions compared to measured data will be discussed in detail.

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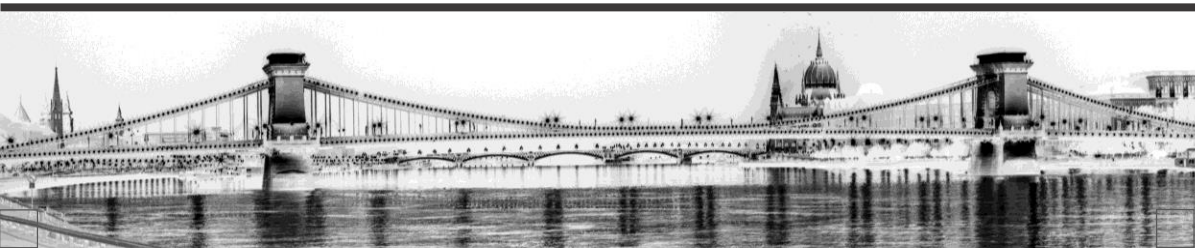

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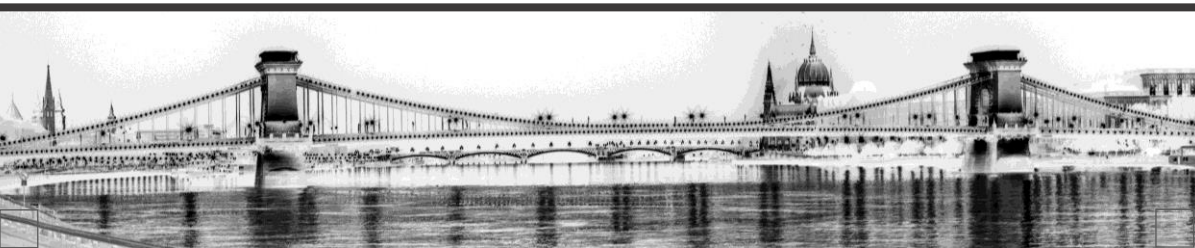
Diffusive Memristors For Computing

In the big data and IoT era, energy efficiency of computing has become an increasingly important and urgent topic. Human brain is known for being very efficient in energy consumption while traditional complementary metal–oxide–semiconductor devices and circuits are inefficient in implementing brain-inspired computing paradigms.[1] Devices that behave more directly like synapses and neurons should enable a significantly more efficient implementation of a neural network. In order to more faithfully emulate (rather than just simulate) actual synapses and neurons, it is crucial for emerging devices to possess diffusive dynamics, which plays critical roles in synaptic and neuronal functions. To emulate the fundamental dynamic process in electronic devices, we developed Ag-in-oxide diffusive memristors[2] with a temporal response during and after stimulation similar to that of ion diffusion dynamics in the biosystems. The diffusive memristor and its dynamics enable a direct emulation of both short- and long-term plasticity of biological synapses and provide a viable solution for the crucial synaptic dynamics in neuromorphic computing.[3] In addition, combined with its intrinsic capacitance, a certain type of diffusive memristor has exhibited Leaky Integration and Fire (LFI) function, making it possible to achieve an artificial neuron using a single highly scalable and stackable emerging nanodevice.[4] An integrate neural network fully based on memristive synapses and neurons was built to demonstrate pattern classification with unsupervised learning.[4] In addition, the diffusive memristors can be used for true random number generators[5] in cybersecurity applications and artificial nociceptors[6] in robotics applications.



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5 Jiang, H. et al. A Novel True Random Number Generator Based on a Stochastic Diffusive Memristor. Nature communications 8, 882 (2017).
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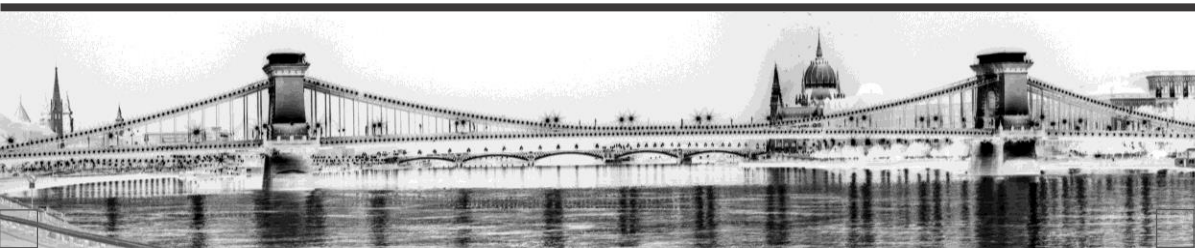
Analog Computing with Networks of Memristors Oscillators

Nonlinear dynamic behavior of memristors is exploited in oscillatory and chaotic circuits. A thorough study is necessary to understand the rich complex nonlinear phenomena emerging in memristor circuits. The aim of this talk is to present a novel systematic methodology for the analysis of a large class of nonlinear circuits containing memristors.
The class is constituted by ideal capacitors, ideal inductors, ideal resistors, ideal independent voltage and current sources, and memristors that are either flux–controlled and/or charge–controlled. The main advantage of the proposed method is that it enables to describe adaptive memristor–based circuits by means of a reduced number of Ordinary Differential Equations compared to current approaches available in literature. This permit to simplify the investigation of nonlinear dynamic behavior and bifurcations without parameters in memristor circuits and to make clear the influence of initial conditions.



Dr. Vikas Rana and Rainer Waser
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Forming Free ReRAM Devices and its application beyond Data Storage

Redox-based resistive random access memory (ReRAM) has shown low power consumption, fast switching speed and ultra-dense integration capability [1]. However, one time electroforming process, that is required to initiate the switching process, consumes more power than that of switching cycles. The higher power consuming step makes these devices incompatible to low-voltage CMOS technology. Therefore, it is important to have forming-free ReRAM devices. We demonstrate the forming free ReRAM devices by ion implantation in the metal oxide thin-film during the device fabrication process. These forming free devices show very high endurance and retention [2]. Besides their potential as memory, ReRAM devices in crossbar configuration offer implementation of memory-intensive computing paradigm and adds an extra edge to this technology. With multi-level switching capability, an intrinsic modular arithmetic using a ternary number system will be presented. This opens up the computing space beyond traditional binary values [3].

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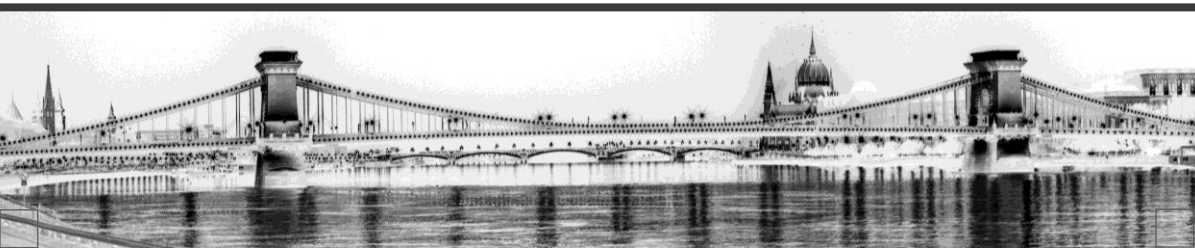

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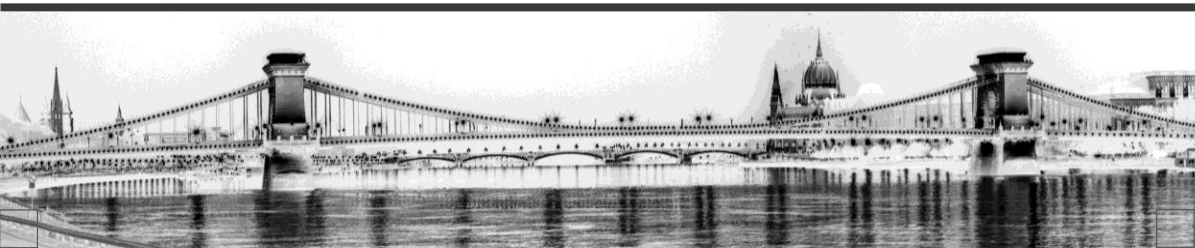
Complex dynamics and multistability in nonlinear electronic circuits and memristive systems

This lecture is devoted to current progress in the the study of complex dynamics and multistability in nonlinear electronic circuits such as Chua circuits, memristive systems, and phase-locked loop-based circuits. The aim is to discuss the modern trends in the development of effective analytical-numerical methods.

In the first part of the lecture, general approaches to the analysis of stability, periodic and chaotic self-excited and hidden attractors in the nonlinear dynamical models of electronic circuits and memristive systems are discussed. While self-excited attractors can be revealed numerically by the integration of trajectories, started in small neighborhoods of unstable equilibria, the hidden attractors have the basins of attraction, which are not connected with equilibria, and for their localization it is necessary to develop special analytical-numerical methods.

The second part of the lecture is devoted to nonlinear analysis of the phase-locked loop-based circuits (PLLs). The classical PLLs are essentially nonlinear control systems with slow-fast dynamics and their rigorous analytical and numerical analysis is a challenging task. We discuss and fill some of the gaps identified between the mathematical control theory and the theory of dynamical systems, on the one hand, and the engineering practice of PLLs, on the other. Effective analytical methods for the estimation of the pull-in and lock-in ranges, corresponding to global stability and acquisition without slipping cycles, are considered.

The material of the lecture is based on the following recent authors' works [1-10].



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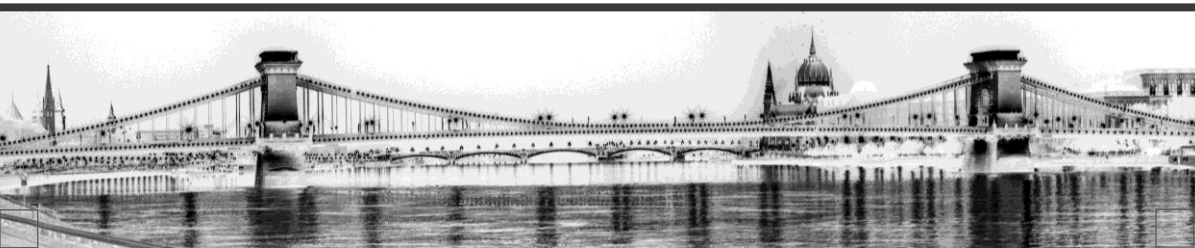

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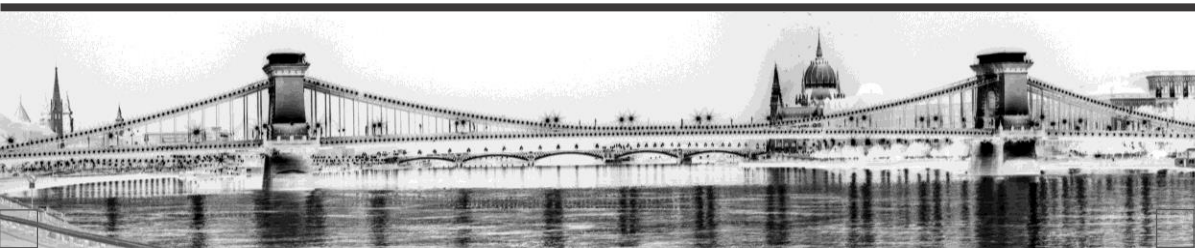
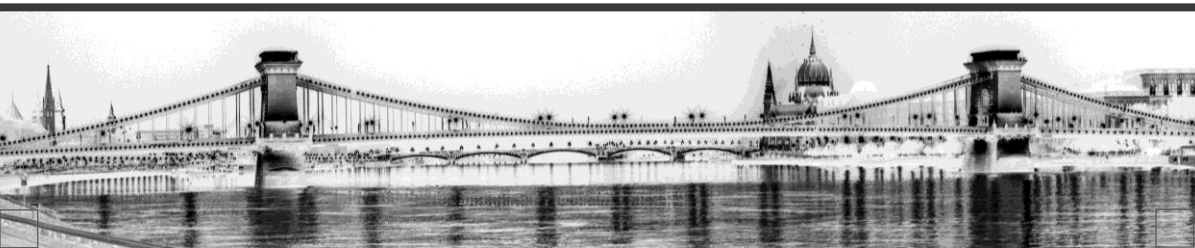
The Memristive Cellular Automata Computing Paradigm: Emergent Applications and Future Trends

In this talk, the notion of memristor device as a fine element for today's ubiquitous computing is coupled with the computational model of Cellular Automata (CAs). Having in mind that in the CAs computational approach, memory and processing are inseparably related to the same unit, i.e. CA cell, the proposed matching with memristors is straightforward and, moreover, quite promising for a number of applications. For example, arriving from computational intelligence, NP and NP-hard problems have become more and more apparent in various real time applications and the need of finding efficient ways for solving such problems is of utter importance. In this talk, we will meticulously discuss and successfully design CA memristor based circuits that are able to solve a variety of such hard computational problems like the Shortest Path, Bin Packing, Knapsack and the Max-clique problem, respectively. More specifically, we present the design of a 2-D CA-based memristive circuit able to detect the nodes belonging to the shortest path solution of a given mesh. Simulations confirm the correct behavior of the proposed CA-inspired circuit for both single source to single destination and also to multiple destinations, also providing a possible solution to the travelling salesman problem by the iterative application of the shortest path solution



process. In addition, we design a CA-inspired circuit that performs both the sorting of a linear array and the solution of classical Bin Packing Problem. For the packing circuit a basic cell was designed to implement the desired 1-D CA rule and then employed in a 2-D computing structure. The resulting 2-D structures implements the “First Fit" Bin Packing algorithm, while a set of simulations took place to ensure the correct behavior for both the sorting and the packing circuits and the resulting solutions of the proposed algorithm were compared with the results of a 1-D Bin Packing Problem benchmark. Using the aforementioned Bin Packing algorithm and circuit as bases, we design a new circuit capable of solving the Knapsack problem, while the results were compared with those from a published benchmark. Moreover, we design a CA based memristive circuit that can be used along with a neural network to provide the solution to the Max-Clique Problem. The CA was chosen to be designed as a memristive based circuit, while the neural network was treated as a “black box”. More eeal applications are considered, and the results of elementary CA modeling and simulation for the generation of pseudo-random numbers are presented using a 1-D memristor-based CA array to illustrate the robustness and the efficacy of the proposed computing approach. Furthermore, a novel memristive Cellular Automata circuit-level approach for the modeling of healthy and pathogenic brain regions during epileptic seizures. The proposed design emulates epilepsy-related phenomena in the brain, exploiting the parallelism of CA and memristor’s dynamics to model a highly scalable network of neurons. Consequently, we expect that in the near future the experimental implementation of such proposed memristive CA structures could be rather helpful for a vast number of applications resulting massively parallel processors or Neuromorphic computing architectures offering new advantages in terms of parallelization, reconfigurability, scalability, power consumption and high computing performance.



Plenary talk

Ángel Rodríguez-Vázquez
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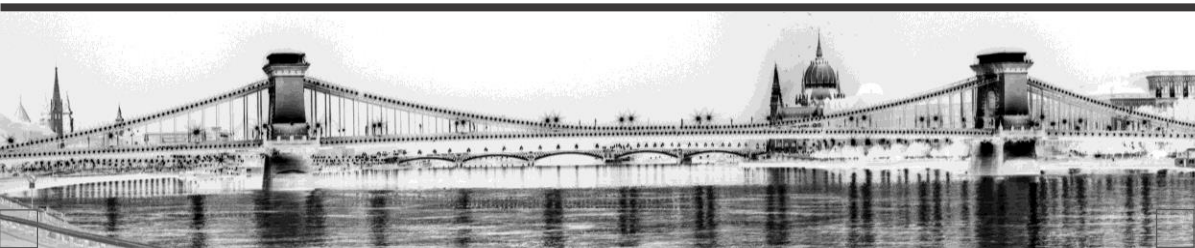
Single Photon Detection in CMOS

Single Photon Avalanche Detectors (SPADS) are receiving significant interest due to their compatibility with mainstream CMOS, their reduced SWaP and their insensitivity to magnetic fields. SPADs can both count single photons and signal the time instances of these counts. On the one hand, heir ability to count single photons makes them suitable for low-light detection. On the other hand, their ability to signal photon counts in time made them suitable for TCSPC techniques. Hence, potential applications of SPAD include surveillance, LIDAR and range-finding, FLIM, PET, and various types of spectroscopy. This lecture overviews architectures and applications of SPAD CMOS imagers and illustrate their challenges and their prospects for industrial usage.

Technical sessions

Technical session 1.1: Beyond Moore implementations: Memristors and Oscillators
Chairman: Valeri Mladenov 10:30-12:50

	AUTHORS	TITLE
10:30	Stanislaw Jankowski, Zbigniew Szymański and Zbigniew Wawrzyniak	Two-dimensional memristive CNN for sequence recognition
10:50	Alon Ascoli, Ronald Tetzlaff, Daniele Ielmini and Leon Chua	Theory of CNNs with hafnium oxide RRAMs
11:10	Valeri Mladenov	Synthesis and Analysis of a Memristor-Based Artificial Neuron
11:30	Rafailia-Eleni Karamani, Iosif-Angelos Fyrigos, Vasileios G. Ntinas, Ioannis Vourkas and Georgios Ch. Sirakoulis	Game of Life in Memristor Cellular Automata Grid



11:50	Francesco Marrone and Fernando Corinto	Tunable Chaos in Memristor Circuits for Pattern Recognition Tasks
12:10	Linda Gong	Ring Oscillators to Model Artificial Neural Networks
12:30	Zachary Hull and Donald Chiarulli	Hierarchical Modeling of Nano-Oscillator Systems

Technical session 1.2: Medical applications

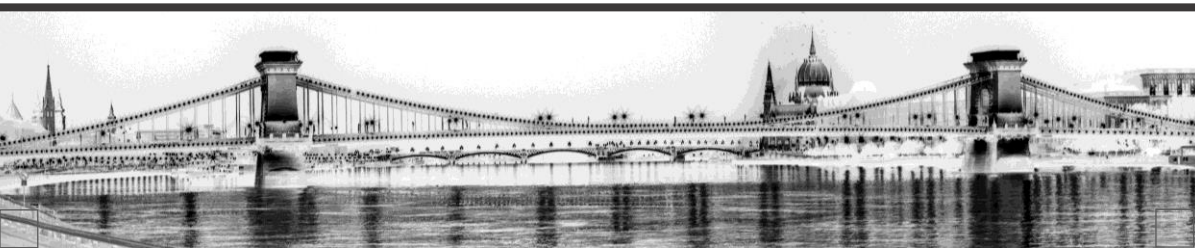
Chairman: Akos Zarandy 14:00-15:40

	AUTHORS	TITLE
14:00	Ioan Buciu, Cristian Grava, Laviniu Telepea and Alexandru Gacsadi	Mammogram Classification with Local Phase Quantization Features
14:20	Maide Bucolo and Fabiana Cairone	Complex Spatio-Temporal Patterns in Red Blood Cells Flows
14:40	Daniel Terbe and Akos Zarandy	Remote camera based measurement of human vital signs
15:00	Orsolya Heri, Antal Hiba and Akos Zarandy	Automatic skin lesion analysis using relatively small learning set
15:20	Yahya Moshaei Nezhad, Jens Müller, Ronald Tetzlaff and Nico Hoffmann	A New Approach for Motion Estimation and Correction of Thermographic Images in Brain Surgery

Technical session 1.3: Cameras, Architectures, and VLSI Implementation

Chairman: Ricardo Carmona 16:00-17:40

	AUTHORS	TITLE
16:00	Selman Ergünay and Yusuf Leblebici	A Smart Camera Architecture with Keypoint Description and Hybrid Processor Population
16:20	Takahisa Ando, Yoko Uwate and Yoshifumi Nishio	Two-Layer Cellular Neural Networks with Layer of Delay Output
16:40	Ari Paasio	Asyncronous Object Center Extraction for Pixel Detectors
17:00	Marco Trevisi, Ricardo Carmona-Galán, Jorge Fernández-Berni and Ángel Rodríguez-Vázquez	1D Cellular Automata for Pulse Width Modulated Compressive Sampling CMOS Image Sensors
17:20	Ari Paasio and Jonne Poikonen	Approximating Binary Object Skeletonization with Pixel-Level Asynchronous Propagation



Plenary talk

Andras Horvath, Akos Zarandy, Peter Szolgay
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From Cellular Neural Networks to Convolutional Neural Networks

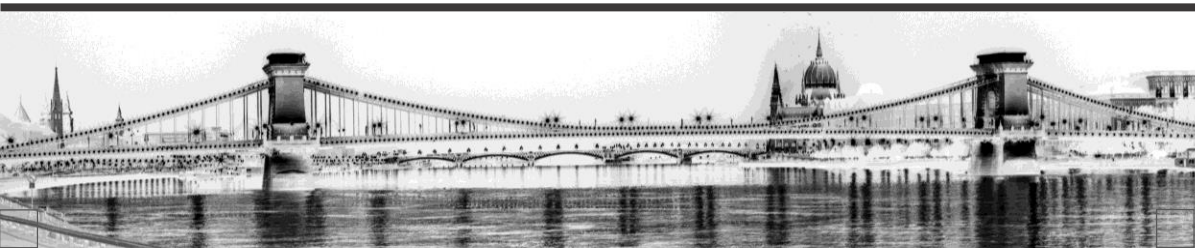
Convolutional Neural Networks became ubiquitous in the past five years and researcher are trying to create more efficient, low energy implementations of these architectures. Cellular Neural Networks offer an easily scalable, analogue, energy-efficient structure, which can exploit the characteristics of current emerging devices. Various theoretical and circuit design approaches were introduced in the field of Cellular Neural Network in the past decade which can be used generally with neural networks providing higher energy efficiency, accuracy or robustness. The talk will focus on these properties and try to illustrate them with a few examples.

Technical sessions

Technical session 2.1: Applications

Chairman: Antal Hiba 10:20-12:00

	AUTHORS	TITLE
10:20	Taishi Iriyama, Masatoshi Sato, Tsuyoshi Otake, Hisashi Aomori and Mamoru Tanaka	Color Filter Array Interpolation Using Cellular Neural Networks Considering Self-Congruence
10:40	Tomohiro Fujita, Masami Nakayama, Takeshi Kumaki and Takeshi Ogura	Cellular Automaton Based Random Noise Generator with Post-Processing for DT-CNN Annealing
11:00	Peter Bauer, Akos Zarandy, Antal Hiba and Jozsef Bokor	Camera-based In-time Detection of Intruder Aircraft
11:20	Antal Hiba, Tamas Zsedrovits, Orsolya Heri and Akos Zarandy	Runway detection for UAV landing system
11:40	Lorant Kovacs, Laszlo Lindenmaier, Huba Nemeth, Viktor Tihanyi and Akos Zarandy	Performance Evaluation of a Track to Track Sensor Fusion Algorithm



Technical session 2.2: FPGA implementation

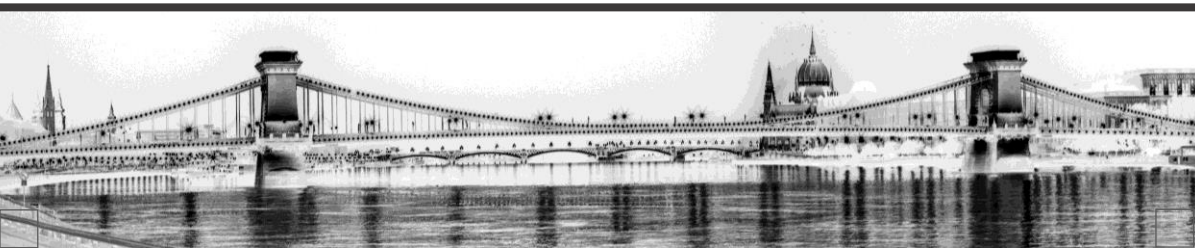
Chairman: Mustak Yalcin 13:10-14:50

	AUTHORS	TITLE
13:10	Daniel Balazs Becker, Istvan Zoltan Reguly and Gihan R. Mudalige	An abstraction for local computations on structured meshes and its extension to handling multiple materials
13:30	Dogancan Davutoglu, Nerhun Yildiz, Vedat Tavsanoglu and Umut Engin Ayten	Real-Time Video Frame Differentiator Based on DDR3 SDRAM Memory Interface
13:50	Andras Kiss, Zoltan Nagy, Levente Mark Santha and Gyorgy Csaba	An Efficient Multi-Level Fast Multipole Method Implementation on FPGA
14:10	Erdem Kose and Mustak Erhan Yalcin	A New Architecture for Emulating CNN with Template Learning on FPGA
14:30	Jens Müller and Ronald Tetzlaff	Comparison of numerical integration methods for digital hardware implementations

Demo Session

Chairman: Alon Ascoli, Zoltan Nagy 14:50-16:00

	AUTHORS	TITLE
1.	Dogancan Davutoglu, Nerhun Yildiz, Vedat Tavsanoglu and Umut Engin Ayten	Demo: Real-Time Video Frame Differentiator Based on External Memory Interface
2.	Akos Zarandy, Daniel Terbe	Photoplethysographic measurements with the Eye-Ris system
3.	Zoltan Nagy	Demo: Multi-channnel mammalian retina model on FPGA
4.	Zoltan Nagy	Demo: Two dimensional supersonic flow simulation



Plenary talk

Wolgang Porod(+) and György Csaba(++)
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Computing with dynamical systems

In this talk, we will discuss an alternative approach to computing. Instead of basing a computer on the manipulation of bits, we will explore the possibility of harnessing dynamical systems for computation. Specifically, we will consider physical processes and dynamical systems based on waves and on coupled oscillators. In such dynamical systems, the computational process more closely exploits the underlying physics, which offers the promise of lower power dissipation.

Technical sessions

Technical session 3.1: Network Theory and Learning

Chairman: Paolo Arena 10:50-12:30

	AUTHORS	TITLE
10:50	Lucia Valentina Gambuzza, Mattia Frasca and Vito Latora	Controlling synchronization of a group of network nodes
11:10	Miklos Koller, Marcell Simko and Barnabas Garay	Dynamics of a Chua-Yang ring network in 8D
11:30	Paolo Arena, Andrea Bonanzinga and Luca Patanè	Role of feedback and local coupling in CNNs for locomotion control of a quadruped robot
11:50	Andras Horvath and Domonkos Abraham	Applying the Standard Non-linearity of Cellular Neural Networks in Convolutional Networks
12:10	Jalal Al-Afandi and Andras Horvath	Application of the Nonlinear Wave Metric for Image Segmentation in Neural Networks